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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,627	08/28/2001	Ki Yong Jeon	P-0251	4513

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EXAMINER	
NGO, NGUYEN HOANG	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,627	JEON, KI YONG	
	Examiner	Art Unit	
	Nguyen Ngo	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5 and 9* is/are allowed.

6)☒ Claim(s) *6,7 and 10-16* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to the amendment of June 30, 2005. All changed made to the Specification, Drawings, and claims have been entered. Accordingly, Claims 1-16 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 6, 7, and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Russell et al. (US 6584118), hereinafter referred to as Russell.

Regarding claim 6, Russell discloses an apparatus comprising methods of mapping Ethernet data frames into SDH virtual containers (serial data mapping apparatus, Abstract). Russell further discloses;

hardware implementation for converting a plurality of serially received 9 bit encoded data blocks (Ethernet data corresponding to asynchronous data) into a plurality of 8 bit bytes suitable for packing into an SDH payload and that a plurality of 9 bit shift registers receive 9 bit encoded data blocks, each of 9 bits size, which output into a plurality of 8 bit shift registers, which feed into an SDH payload and that the 8 bit shift registers is then unloaded into an SDH payload (a plurality of elastic buffers (shift registers), each buffer receiving serial asynchronous data (9 bit blocks), and outputting parallel data bits as byte units (8 bit bytes) of the asynchronous data, col12 lines 24-42).

of an SDH mapper that maps Ethernet data frames (asynchronous data) directly into SDH data frames (a virtual container mapper unit that maps the byte units to a virtual container signal, col7 lines 54-57). It should be obvious that this SDH mapper incorporates the shift registers as mentioned above to map the frames (asynchronous data) into SDH data frames (virtual containers).

Regarding claim 7, Russell discloses that a set of STM frames are assembled to contain a plurality of virtual containers which are carried as an STM-N payload (col7 lines 66-col8 lines2) and that an Ethernet port card is incorporated into a SDH multiplexer, so that as well as having a plurality of tributary interfaces, for example STM-1, the multiplexer also has an interface for frame based data systems (comprising an STM-1 formatter that multiplexes the virtual container signal as an STM-1 signal, col7 lines19-25).

Regarding claim 13, Russell discloses of methods of mapping Ethernet data frames into SDH virtual containers (a method of mapping serial data, Abstract). Russell further discloses;

hardware implementation for converting a plurality of serially received 9 bit encoded data blocks (Ethernet data corresponding to asynchronous data) into a plurality of 8 bit bytes suitable for packing into an SDH payload and that a plurality of 9 bit shift registers receive 9 bit encoded data blocks, each of 9 bits size, which output into a plurality of 8 bit shift registers, which feed into an SDH payload and that the 8 bit shift registers is then unloaded into an SDH payload (receiving each of a plurality of serial asynchronous data signals into a plurality of elastic buffers (9 bit data blocks into shift registers) and reading a parallel asynchronous signal of 8 bits as a parallel data byte unit (8 bit bytes suitable for packing into an SDH payload from shift register), col12 lines 24-42).

of an SDH mapper that maps Ethernet data frames (asynchronous data) directly into SDH data frames (multiplexing parallel data units read from the plurality of elastic buffers into a virtual container singal, col7 lines 54-57).

that a set of STM frames are assembled to contain a plurality of virtual containers (SDH data frames) which are carried as an STM-N payload (col7 lines 66-col8 lines2) and that an Ethernet port card is incorporated into a SDH multiplexer, so that as well as having a plurality of tributary interfaces, for example STM-1, the multiplexer also has an interface for frame based data systems (generating an STM-1 signal from the virtual container signal, col7 lines19-25).

5. Claims 10, 11, 12, 14, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russell et al (US 6584118) in view of Ha et al. (US 5933432) hereinafter referred to as Russell and Ha.

Regarding claim 10, Russell fails to disclose the specific limitations of claim 10, more specifically of having a system clock that controls the timing.

Ha however discloses that in asynchronous mapping, since the clock frequency of received data is different from that of the sending data, errors may occur (col1 lines 39-43), thus providing the motivation of incorporating a clock signal into a SDH mapper to decrease errors. Ha further discloses of an DS clock that is provided to the write address generator which provides a write address for each bit of the DS data to the buffer based on the DS data (system clock that controls the timing of writing the asynchronous data to the plurality of elastic buffers, col3 lines 29-33) and a V5 clock for initiating the formation of a VC (system clock that controls reading the parallel data bits to the virtual container mapper unit).

It should thus be obvious to a person skilled in the art to incorporate clock pulses as disclosed by Ha into the method of mapping Ethernet data frames into virtual containers as disclosed by Russell in order to decrease an errors in data processing and transmission.

Regarding claim 11, Russell discloses;

that a set of STM frames are assembled to contain a plurality of virtual containers (containing Ethernet frames corresponding to DS signals) which are carried as an STM-N payload (col7 lines 66-col8 lines2) and that an Ethernet port card is incorporated into a SDH multiplexer, so that as well as having a plurality of tributary interfaces, for example STM-1, the multiplexer also has an interface for frame based data systems (STM-1 formatter that multiplexes the virtual container as an STM-1 signal and multiplexes the virtual container having portions of the DS-1 and DS-1E signals into the STM-1 signal, col7 lines19-25).

of an SDH mapper that maps Ethernet data frames (DS-1 and DS1E signals) directly into SDH data frames (a virtual container mapper unit that maps portions of the plurality of DS-1 and DS-1E signals (bits) into the virtual container signal, col7 lines 54-57).

Russell however fails to disclose the limitation of having a read pointer generating unit that generates the read addresses.

Ha however discloses from figure 2 of a read address generator and the means for generating a read address signal for reading the stored digital signal data in response to the read address signal to provide the digital signal data mapped into a virtual container (a read pointer generating unit the generates the read addresses for a plurality of DS-1 signals and a plurality of DS-1E asynchronous signal received, col8 lines 9-16) and thus provides the motivation to incorporate a read address generator to

efficiently distinguish the start of the mapping of a data frame into a SDH data frame from a buffer.

It would thus be obvious to a person skilled in the art to incorporate the read address generator as disclosed by Ha into the method of mapping Ethernet data frames into virtual containers as disclosed by Russell in order to efficiently read out stored digital data (Ethernet data frame) from buffers into a SDH data frame.

Regarding claim 12, Russell and Ha disclose all the limitations of claim 12. More specifically Ha discloses of an DS clock that is provided to the write address generator which provides a write address for each bit of the DS data to the buffer based on the DS data (system clock that controls the timing of writing the asynchronous data to the plurality of elastic buffers, col3 lines 29-33) and a V5 clock for initiating the formation of a VC (system clock that controls reading the parallel data bits (plurality of DS-1 and DS-1E signals) to the virtual container mapper unit).

Regarding claim 14, Russell fails to disclose the specific limitations of claim 14, more specifically the generated read addresses, generated write addresses, and system clock controls.

Ha however discloses from figure 2;

of a read address generator and the means for generating a read address signal for reading the stored digital signal data in response to the read address signal to provide the digital signal data mapped into a virtual container (reading the parallel data units from the plurality of elastic buffers, according to generated read addresses, col8 lines 9-16).

of a write address generator and the means for generating a write address signal for storing the digital signal data in response to the write address signal (writing the plurality of serial asynchronous data signals to the plurality of elastic buffers, according to generated write addresses, col7 lines20-23).

of a DS clock that is provided to the write address generator which provides a write address for each bit of the DS data to the buffer based on the DS data (system clock that controls the timing of writing the asynchronous data to the plurality of elastic buffers, col3 lines 29-33) and a V5 clock for initiating the formation of a VC (system clock that controls reading the parallel data bits to the virtual container signal).

It should thus be obvious to a person skilled in the art to incorporate a read address generator, write address generator, and clock signals as disclosed by Ha into the method of mapping Ethernet data frames into virtual containers as disclosed by Russell in order to efficiently read out stored digital data (Ethernet data frame) from buffers into a SDH data frame with little error.

Regarding claim 15 and 16, Russell and Ha disclose all the limitations of claim 15 and 16. As seen in figure 2 disclosed by Ha, there are only one write and read address generators and correspondingly, Russell discloses of a plurality of shift registers (which would be obvious to be incorporated into the 220 buffer (220 of figure 2 of Ha) and thus it is obvious that the number of read and write pointer generators (pointer generating units) is less then the number of shift registers (plurality of elastic buffers).

Allowable Subject Matter

6. Claims 1-5 and 9 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

7. Claim 1 is are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose **a VC mapping unit that maps a DS asynchronous signal to a VC signal as a byte unit, according to the mapping address and wherein the VC mapping unit comprises a plurality of elastic buffers that write the DS asynchronous signal as a bit unit and read the DS asynchronous signal as the byte unit comprising a parallel asynchronous signal of 8 bits.** It is noted that the closest prior art, Russell et al. (US 6584118) discloses the method of mapping Ethernet data frames into SDH virtual container. However, Russell fails to disclose or render obvious to the above underline limitations as claimed.

8. Claim 9 is are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose **that the read pointer**

generating unit increments or decrements the read address, after each of a number of the parallel data bits is read from the elastic buffer, by a value of four, six, or eight, and the value by which the read pointer generating unit is incremented or decremented depends on a number of null bits received in the serial asynchronous data. It is noted that the closest prior art, Russell et al. (US 6584118) discloses the method of mapping Ethernet data frames into SDH virtual container. However, Russell fails to disclose or render obvious to the above underline limitations as claimed.

9. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. This claims is allowable due to the further limitations claim 8, more specifically of a virtual container framer that identifies a mapping position of the asynchronous signal, based on the mapping address generated by the STM-1 address generating unit, and controls the multiplexing of the number of byte units into the virtual container.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Roberts et al. (US 2002/0159473), Mapping Arbitrary Signals.

b) Ryan et al. (US 6628651), Communication Switching Techniques With Improved Frame Format.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen Ngo whose telephone number is (571) 272-8398. The examiner can normally be reached on Monday-Friday 7am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N.N.
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